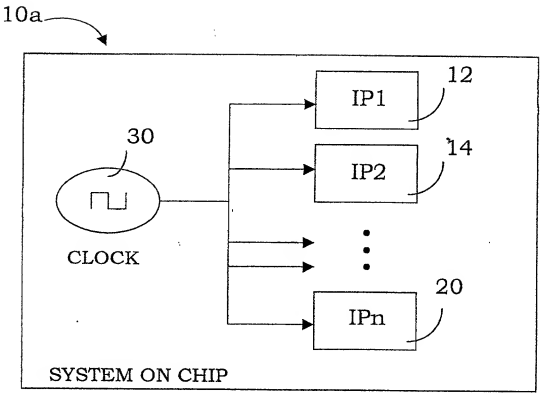

FIG. 1

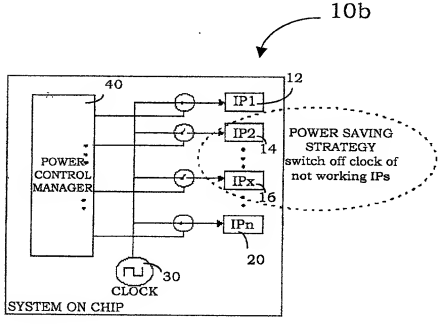

FIG. 2

T05OFT-J10070728

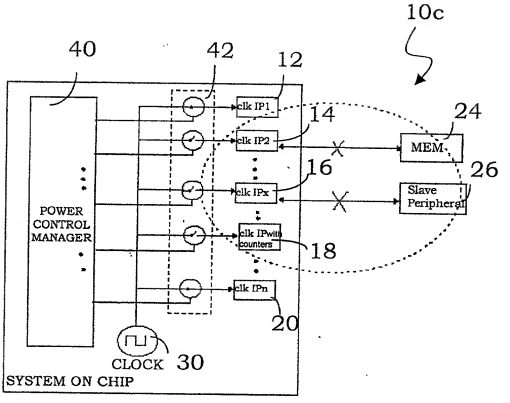

FIG. 3

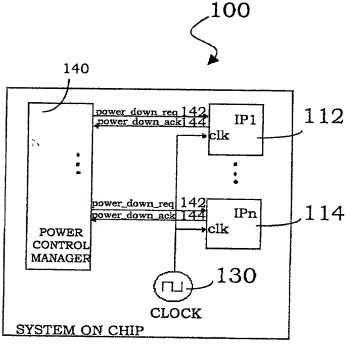

FIG. 4

T0507T "82/07007

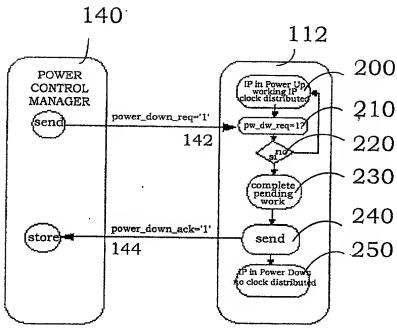

FIG. 5

190

```
Power Down Manager:
        sent to the IP the power_down_req signal set to '1';

IP:
        IF power_down_req is asserted (='1'):
                complete its pending work;
                set power_down_ack to '1';
                stop its own clock => IP halted;
        else
                normal work;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 6

FOUNDATION

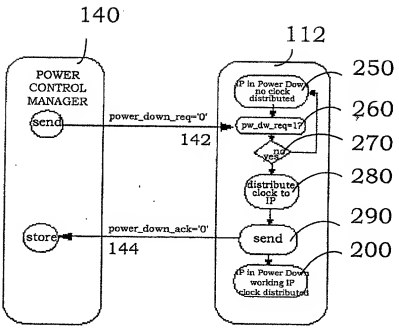

FIG. 7

194

```
Power Down Manager:
        sent to the IP the power_down_req signal set to '0';

IP:
        IF power_down_req is de_asserted (='0'):
                restarts its own clock;
                set power_down_ack = '0';
                restart to work;
        else
                no clock distributed to IP => IP halted;

Power Down Manager:
        Stores the value of power_down_ack to allow visibility
        of IP status (power on/off);
```

FIG. 8

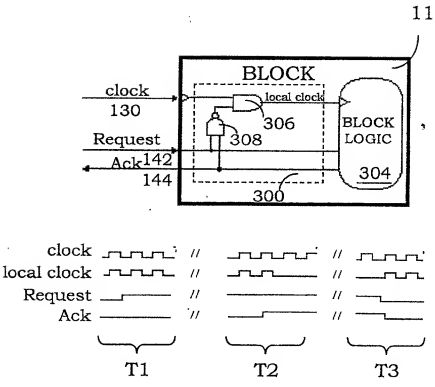
112
BLOCK
clock
130
local clock
306
BLOCK
LOGIC
Request
308
Ack
142
144
304
300
clock
local clock
Request
Ack
T1
T2
T3

FIG. 9

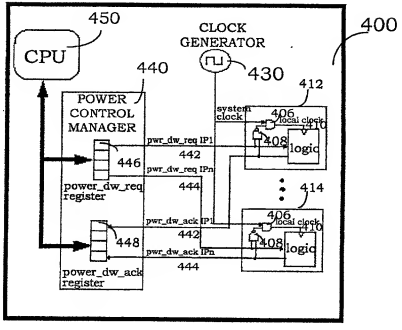
450
CPU
CLOCK
GENERATOR
400
440
430
412
POWER
CONTROL
MANAGER
system
clock
406
local clock
410
408
logic
pwr_dw_req IP1
442
pwr_dw_req IPn
446
power_dw_req
register
444
414
pwr_dw_ack IP1
pwr_dw_ack IPn
448
power_dw_ack
register

FIG. 10